REMARKS

This application has been carefully reviewed in light of the Office Action dated October 21, 2005. Claims 1 to 11 remain in the application. Claim 1 is the independent claim herein. Reconsideration and further examination are respectfully requested.

Claim 1 was objected to for an informality, and Claims 2 to 11 were objected to for being dependent therefrom. In this regard, Claim 1 has been amended giving due regard to the objection raised in the Office Action. Withdrawal of this objection is therefore respectfully requested.

Claims 4 to 5 and 8 to 10 were rejected under 35 U.S.C. § 112, second paragraph, for alleged indefiniteness. Without conceding the correctness of the rejection, Claims 4 to 5 and 8 to 10 have been amended so as to specify the invention with greater clarity. Reconsideration and withdrawal of this rejection are therefore respectfully requested.

Claims 1, 3 and 7 were rejected under 35 U.S.C. § 102(e) over U.S. Patent No. 6,636,927 (Peters). Claims 2 and 11 were rejected under 35 U.S.C. § 103(a) over Peters in view of U.S. Patent Application Publication No. 2003/0233492 (Schelling). Claims 4 to 6 were rejected under § 103(a) over Peters in view of U.S. Patent No. 5,522,055 (Kamanaka), and Claims 9 to 10 were rejected under § 103(a) over Peters in view of U.S. Patent No. 6,587,920 (Mekhiel). Reconsideration and withdrawal of these rejections are respectfully requested.

The present invention generally concerns a memory control apparatus which performs a reading operation on a memory device at a request of a plurality of masters. A

read means pre-reads data subsequent to data which any of the plurality of masters requests to read. A specific master is set among the plurality of masters. A control means determines whether or not a present master which issues a read request is the specific master when the read request is issued from the present master. Among its many features, the present invention includes (i) storing a result of the pre-reading in a prefetch buffer when it is determined that the present master which issues a read request is the specific master, and (ii) refraining from changing the content of the prefetch buffer when it is determined that the present master is not the specific master.

Referring specifically to claim language, independent Claim 1 as amended is directed to a memory control apparatus which performs a reading operation on a memory device at a request of a plurality of masters. The apparatus includes read means for pre-reading data subsequent to data which any of the plurality of masters requests to read, and a prefetch buffer for holding a result of the pre-reading. The apparatus also includes set means for setting a specific master among the plurality of masters. Additionally, the apparatus includes control means for determining whether or not a present master which issues a read request is the specific master set by the set means when the read request is issued from the present master, storing a result of the pre-reading in the prefetch buffer when it is determined that the present master is the specific master, and refraining from changing the content of the prefetch buffer when it is determined that the present master is not the specific master.

In contrast, the applied art is not seen to disclose or suggest at least the features of (i) storing a result of pre-reading in a prefetch buffer when it is determined that the present master which issues a read request is the specific master, and (ii) refraining

from changing the content of the prefetch buffer when it is determined that the present master is not the specific master.

As understood by Applicant, Peters discloses a bridge device for transferring data using master-specific prefetch sizes. The bridge device is coupled between a first bus and a second bus with the master devices being coupled to the first bus and slave devices being coupled to the second bus. Bridge control circuitry receives a first data request from a selected master device for transferring data between the selected master device and a selected slave device. The circuitry issues a second data transfer request to the selected slave device for transferring the data, which is then stored in a prefetch buffer. The circuitry transfers the stored data from the prefetch buffer to the destination device when the prefetch buffer receives and stores data in a size that corresponds to the prefetch size stored in a prefetch control register associated with the selected master device. See Peters, Abstract.

Pages 4 and 5 of the Office Action assert that Peters (Column 6, line 66 to Column 7, line 6 and Column 9, lines 11 to 16) discloses control means for determining whether or not the master which issues a request is a master set by the set means when the read request is issued from any of the plurality of masters, and storing a result of a pre-reading in a prefetch buffer when it is determined that the master which issues the request is a master set by the set means.

However, Peters is not seen to disclose or suggest at least the features of (i) storing a result of the pre-reading in a prefetch buffer when it is determined that the present master which issues a read request is the specific master, and (ii) refraining from changing the content of the prefetch buffer when it is determined that the present master is not the

specific master.

In particular, the portions of Peters cited by the Office Action simply describe an arbiter which evaluates bus access requests from one or more PCI devices and grants the PCI bus to one of the requesting PCI devices as a bus master. See Peters, Column 6, line 66 to Column 7, line 7. The bus master device selected by the arbiter makes a data request, and the requested data is received from the host device and stored in the internal prefetch buffer. When the buffer receives data matching the specified prefetch size associated with the selected master device, the data is transferred from the prefetch buffer to the destination device. See Peters, Column 9, lines 11 to 16.

However, Peters is not seen to disclose any determination of whether the device sending a read request is a specific master, much less storing the result of a pre-reading in a prefetch buffer when it is determined that the present master which issues a read request is the specific master. In particular, once a device in Peters "wins" the arbitration, the device can request data to be stored in the buffer, regardless of which device it is. See Peters, Figure 5 and Column 4, lines 28 to 40. Therefore, any determination of access to write to the buffer in Peters is based on the arbitration, which itself takes place before any data requests are sent. See Peters, Figure 5 and Column 8, line 53 to Column 9, line 17. Peters is therefore not seen to make any distinction between which device is currently sending it a data request, as the system of Peters simply accepts and executes data requests from whichever device previously was selected by the arbitration.

Similarly, Peters is not seen to disclose refraining from changing the content of the prefetch buffer when it is determined that the present master is not the specific

master. As stated above, access to the buffer is based on which device wins the arbitration, rather than which device is sending a data request.

In fact, rather than restricting buffer write access to any specific device, Peters indicates that more than one device may be able to write to the buffer at the same time. Specifically, Peters recites that "a transfer to the buffer may begin while another that fills the prefetch buffer is still in progress based on the programmed prefetch size." See Peters, Column 9, lines 17 to 20.

Accordingly, Peters is not seen to disclose or suggest at least the features of (i) storing a result of the pre-reading in a prefetch buffer when it is determined that the present master which issues a read request is the specific master, and (ii) refraining from changing the content of the prefetch buffer when it is determined that the present master is not the specific master.

Schelling, Kamanaka, and Mikheil have been reviewed and are not seen to remedy the foregoing deficiencies of Peters.

Accordingly, independent Claim 1 is believed to be allowable over the applied references. Reconsideration and withdrawal of the § 102(e) rejection of Claim 1 is therefore respectfully requested.

The other claims in the application are each dependent from Claim 1 and are therefore believed to be allowable over the applied references for at least the same reasons. Because each dependent claim is deemed to define an additional aspect of the invention, however, the individual consideration of each on its own merits is respectfully requested.

No other matters being raised, the entire application is believed to be in condition for allowance and such action is respectfully requested at the Examiner's earliest

convenience.

Applicants' undersigned attorney may be reached in our Costa Mesa, California office at (714) 540-8700. All correspondence should continue to be directed to our below-listed address.

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